8 GHZ LOW NOISE BIAS TUNED VCO

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ABSTRACT

Design and performance of an 8 GHz cavity stabilized silicon bipolar transistor voltage controlled oscillator is presented. Very linear electronic frequency tuning with minimal output power variations are achieved without voractor by means of the transistor bias control. The VCO is mechanically tuned over 1 GHz frequency range with dialectric tuner. It delivers 50 mW of output power with 17% transistor efficiency and phase noise of -60 dBc/Hz at 1 kHz from carrier.

INTRODUCTION

Electronic tuning of cavity stabilized oscillator is usually accomplished by means of varactor diode coupled to the cavity. Less known method of electronic frequency tuning is bias tuning, which uses bias dependence of intrinsic transistor parameters. Properly chosen simultaneous control of the transistor current J_E and voltage V_{CB}, in opposite directions, result in a very linear frequency tuning, while the oscillator output power is almost constant. Bias tuning requires transistors capable of delivering output power exceeding the required oscillator output by a few dB. Transistor bias may also be used for electronic output power adjustment by changing J_E and V_{CB} in the same direction. Advantage of bias tuning is great simplicity with resulting reliability and low cost.

This paper presents 8 GHz, cavity stablilized, bias tuned, bipolar transistor VCO design consideration and test results. Packaged grounded-collector transistor was used to generate 50 mW of output power with 17% transistor efficiency at 8 GHz. The VCO is mechanically tuned between 7.5 and 8.5 GHz with dielectric tuner. Mechanical tuning sensitivity does not exceed 100 MHz/turn. The stabilizing cavity is made of aluminum and is partially compensated to reduce the frequency drift with temperature to below 6 MHz between 0°C and +50°C. The electronic tuning range is 15 MHz minimum over entire mechanical tuning range. This is adequate to maintain the VCO frequency locked over expected changes due to temperature, humidity and aging. The free run VCO phase noise density is -60 dBc/Hz at 1 kHz and -90 dBc/Hz at 10 kHz from the carrier.

Initial application of the VCO is in the PLL LO used on the 8 GHz long haul 90 mB/s digital radio.

VCO DESIGN

Bipolar transistors for microwave applications are packaged in common collector configuration to facilitate heat transfer from the transistor chip to the outside world. Fig. 1 shows the cross section of such transistor package, with visible imbeding of the chip in copper flange. The base collector port is coupled to the cavity, which defines the oscillator frequency.

The transistor behaves like negative resistance parallel with bias dependent reactance. The negative resistance is a result of the internal transistor feedback. This feedback can be optimized by addition of external reactance X_{EC}. Capability of the transistor to generate negative resistance can be evaluated from stability circles. S parameters of the device selected for this design and calculated stability circles in Z_{EC} plane are given in Table 3. The circuit can oscillate when the Z_{EC} impedance is in the unstable region outside of the stability circle for given frequency. The amplitude of oscillation is maximized when the magnitude of the transistor reflection coefficient is maximized.

Fig. 2 shows the transistor base-collector reflection coefficient as function of the reactance terminating the emitter-collector port. Above 6 GHz the transistor requires inductive reactance in emitter. Value of the optimum reactance falls down with frequency. Simultaneous optimization of the transistor reflection coefficient at different frequencies is not possible since all real life reactances are growing fuctions of frequency. However by optimizing the emitter reactance at high frequency the transistor reflection coefficient and consequently the oscillator output power variation with frequency can be minimized. This technique plus frequency dependent output load coupling was used to achieve almost constant output power over 1 GHz frequency range.

Details of the electronic frequency tuning are given in Fig. 3 and Fig. 4. Two intrinsic transistor parameters playing major part in bias tuning are identified. The emitter junction

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resistance R_E is controlled by emitter current and the collector junction capacitance C_C is controlled by collector-base voltage. From Fig. 3 one can make general conclusions that the oscillator frequency would be tuned down by rising emitter current and up by rising collector-base voltage.
Analysis of the bias tuning is complicated by many unknowns in the presented equivalent circuit. The analysis based on S parameters would require accurate measurement of S parameters versus frequency, emitter current and V_{CB} voltage plus model of the cavity with the transistor and output coupling structures. Bias tuning was analyzed empirically on 8 GHz oscillator with results presented in Fig. 5. The transistor-cavity coupling affects strongly the electronic tuning sensitivity but not the shape of the presented curves.

The transistor is biased at mid point of the electronic tuning range, which coincides with minimum output power variation versus control voltage and maximum transistor efficiency. Fig. 6 shows measured oscillator frequency and output power versus the frequency control voltage.

The cavity was designed for high Q, low microphonic sensitivity and low cost. The measured unloaded Q of the cavity was 3500. Dilectric tuner was used to achieve smooth, low sensitivity non-erratic tuning.

VCO PERFORMANCE

Measured performance of the 8 GHz VCO is given in Figures 7 and 8. Output power was measured after isolator (0.5 dB loss) at room temperature with frequency control voltage at mid range. Very flat + 17 dBm minimum output power over 1 GHz mechanical tuning range is the result of inductive emitter loading and frequency sensitive output coupling.

Electronic tuning range was measured for frequency control voltage varying between 0 and -12V. Output power variation over electronic tuning range did not exceed 0.5 dB. 15 MHz minimum of electronic tuning is adequate to compensate frequency drift due to temperature, humidity and aging. The temperature related VCO frequency drift is partially compensated by dielectric tuner, mostly at low frequencies.

VCO phase noise was measured on HP3047A spectrum analyzer system. The noise shown in Fig. 8 is a sum of the free run VCO noise and the phase locked VCO noise. Approximately 3 dB contribution of the PLL VCO noise is visible above 5 kHz. The free run VCO noise close to the carrier has 30 dB-/decade flicker FM noise characteristic. Measured phase noise is -30 dB/Hz at 100 Hz, -60 dBC/Hz at 1 kHz and -90 dBC/Hz at 10 kHz from carrier.

The microwave transistor is conservatively biased at 50% of its rated voltage and current. The operating junction temperature at + 25°C ambiant temperature does not exceed + 60°C, which assures very high VCO reliability.

CONCLUSIONS

A low noise cavity stabilized bias tuned voltage controlled oscillator has been described. Commercially available packaged bipolar transistor was used for both RF power generation and electronic frequency tuning. The performance reported does not represent the ultimate in bipolar transistor oscillator performance. Higher frequency, higher power and lower noise are achievable. The design combines good performance with great simplicity, low cost and high reliability.

ACKNOWLEDGMENT

The author is grateful to W. Przewlocki for all help and constant encouragement and to L. Duque for assistance in measurements.

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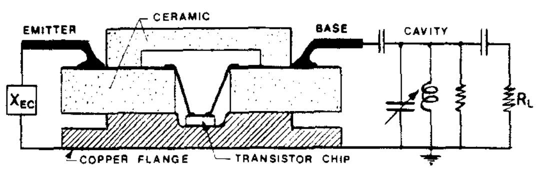

Figure 1 Cross section of the oscillator transistor package and its RF connections in the oscillator circuit.

S Parameters

F MHz	S11		S21		S12		S22	
7000	.69	130	.91	- 157	.86	- 87	.36	- 2
8000	.65	105	.83	- 175	.87	- 115	.30	- 20
9000	.68	74	.72	162	.85	- 137	.26	- 33

Stability Circles in Z_{EC} Plane

	Location			
F MHz	Magn.	Angle	Radius	Stable
7000	4.33	12	4.68	Inside
8000	3.23	31	3.66	Inside
9000	4.24	45	4.70	Inside

Table 1 Transistor S Parameters and Stability circles.

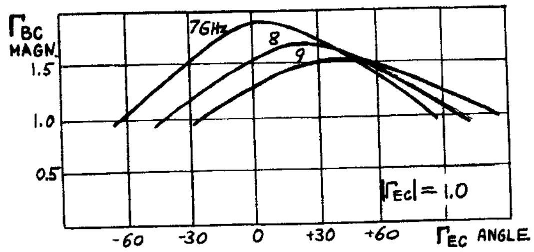

Figure 2 Base Collector Reflection Coefficient versus reactance terminating the emitter -collector port

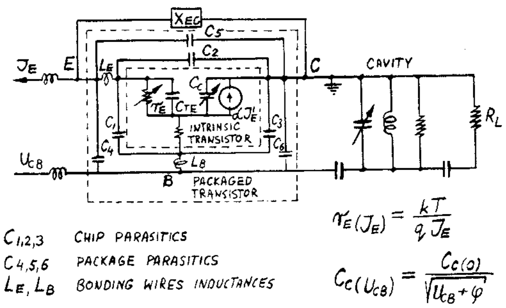

Figure 3 Simplified Equivalent circuit of the Microwave bipolar transistor with identified bias dependant components.

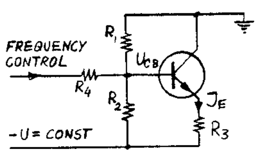

Figure 4 Transistor DC biasing for linear frequency tuning with flat output power.

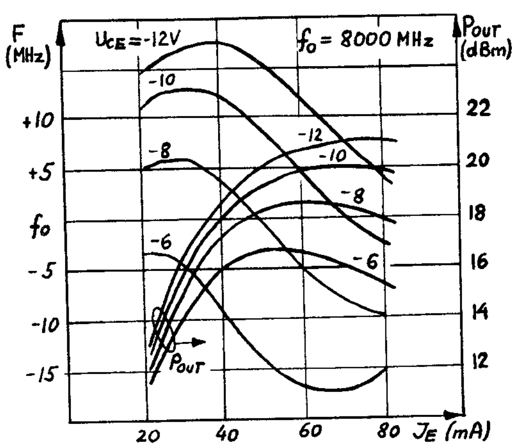

Figure 5 8 GHz cavity stabilized oscillator frequency and output power versus transistor bias.

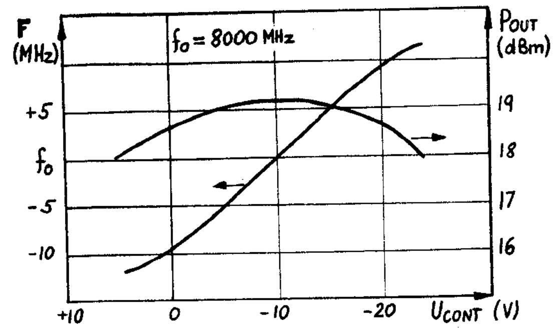

Figure 6 Oscillator Frequency and output power versus control voltage.

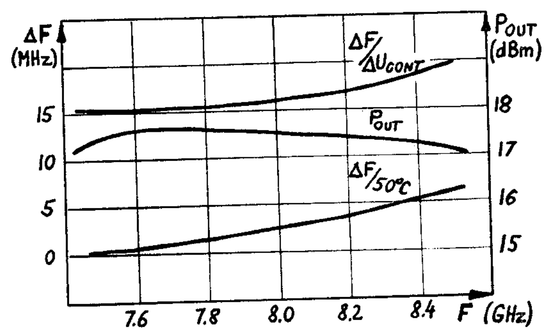

Figure 7 VCO electronic tuning range, frequency drift over 50°C temperature change and output power versus mechanically tuned frequency.

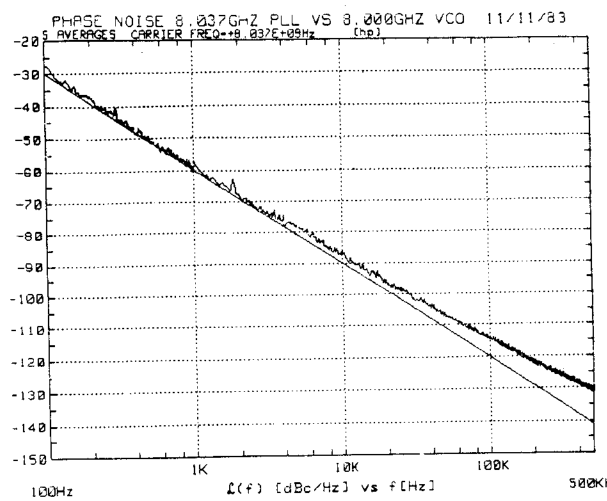

Figure 8 Phase noise of the free run VCO mixed with phase locked VCO (Fn = 5 kHz).